#22/appeal Brief mail 4/21/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicants: | Tinku Acharya, et al. | § | Group Art Unit: | 2625 |
| Serial No.: | 09/390,255 | § | | |
| | | § | Examiner: | Timothy M. Johnson |
| Filed: | September 3, 1999 | § | | |
| For: | Wavelet Zerotree Coding of Ordered Bits | § | Atty. Dkt. No.: | ITL.0210US (P7057) |

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated November 25, 2003, finally rejecting claims 16-33.

## I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010390/0133.

## II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit: January 29, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313.

Janice Munoz

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## III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-15. Subsequently, during prosecution, claims 16-33 were added by amendment. Claims 16-33 have been finally rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

## IV. STATUS OF AMENDMENTS

There are no unentered amendments.

## V. SUMMARY OF THE INVENTION

Referring to Fig. 2, an embodiment 119 of a compression program in accordance with the invention may cause a processor 112 to encode wavelet coefficients in a bit-wise fashion. In this manner, instead of classifying the wavelet coefficients (as zerotree roots or isolated zeros, as examples), the processor 112 may produce codes to classify the bits of the wavelet coefficients. For example, in some embodiments, the processor 112 may classify a particular bit as being either a zerotree root, an isolated zero, a positive node or a negative node. Unlike conventional zerotree coding schemes, thresholds are not computed to identify insignificant values, as the "0" bit is treated as being insignificant and the "-1" and "1" bits are treated as being significant. Specification, pp. 4-5.

In this manner, the processor 112 may generate one of the following codes to classify a particular bit: a "P" code to indicate a positive node if the bit indicates a "1"; an "N" code to indicate a negative node if the bit indicates a "-1"; an "R" code to indicate that a "0" bit is a zerotree root ; and an "IZ" code to indicate that a "0" bit is an isolated zero. In some

embodiments, a particular bit is classified as a negative node only if the bit is the most significant nonzero bit and the bit indicates a "-1." For example, for a coefficient of "-3" that is represented by the three bits "-011," the processor 112 generates an N code to represent the middle bit. However, for this example, the processor 112 generates a P code to represent the least significant bit. Specification, p. 5.

For purposes of providing the wavelet coefficients, the processor 112 may, via wavelet transformations, decompose coefficients that represent pixel intensities of an original image. These wavelet coefficients, in turn, form subbands that are located in multiple decomposition levels. To classify the bits, the processor 112, in some embodiments, may execute the program 119 to process the bits based on their associated bit position, or order. In this manner, the bits of each bit order form a hierarchical tree that the processor 112 may traverse to classify each of the bits of the tree as being either a zerotree root, an isolated zero, a negative node or a positive node. Thus, as an example, the most significant bits of the wavelet coefficients(this bit may also be zero) are associated with one hierarchical tree (and one bit order), and the next most significant bits are associated with another hierarchical tree (and another bit order). Specification, p. 5.

For example, if the absolute maximum wavelet coefficient is represented by three bits (as an example), then all of the wavelet coefficients may be represented by three bits. Therefore, for this example, three hierarchical trees are formed. In this manner, the processor 112 produces a code for each bit based on its indicated value (i.e., "-1," "0," or "1") and possibly (if the bit indicates a "0") its position in the associated hierarchical tree. Specification, p. 5.

In some embodiments, the processor 112 indicates the P, N, IZ and R codes via a bit stream that progressively indicates a more refined (i.e., a higher resolution) version of the original image over time. For example, the processor 112 may use the bits "00" to indicate the "P" code, the bits "01" to indicate the "N" code, the bits "10" to indicate the "R" code and the bits "11" to indicate the IZ code. Other coding schemes are possible. The progressive nature of the bit stream is attributable to the order in which the processor 112 processes the bit orders. For example, in some embodiments, the processor 112 may process the bit orders in a most significant first fashion. Therefore, the processor 112 may initially produce code for all the bits that have the highest bit order, then produce code for all of the bits that have the next highest bit order, etc. As a result of this progressing coding, the resultant bit stream may initially indicate a coarser version of the original image. However, more refinements to the image are indicated by the bit stream over time, as the processor 112 produces the codes for the bits having the lower bit orders. Thus, in some embodiments, the resolution of the image that is indicated by the bit stream improves over time, a feature that may be desirable for bandwidth-limited systems. As a result, a decrease in resolution of the reconstructed image may be traded for a decrease in communication bandwidth. Specification, p. 6.

Referring to Fig. 3, in some embodiments, the processor 112 process the bits of each order in a predefined sequence. For example, for a particular bit order, the processor 112 may begin with the highest decomposition level and produce codes for the bits of the highest decomposition level before proceeding to produce codes for the bits of the next highest decomposition level. The processor 112 produces code(s) for the bit(s) of the LL subband and,

then for each decomposition level, produces code(s) for the bit(s) of the LH subband, subsequently, produces code(s) for the bit(s) of the HL subband and lastly, produces code(s) the bit(s) of the HH subband. Specification, p. 6.

As an example, the wavelet coefficients produced by a two level decomposition may be arranged in a matrix 40 that is depicted in Fig. 4. In this manner, the matrix 40 may be viewed as being subdivided into four quadrants 30a, 30b, 30c and 30d. The upper right 30b, lower left 30c and lower right 30d quadrants includes the coefficients for the LH, HL and HH subband images, respectively, of the first decomposition level. The coefficients for the LL, LH, HL and HH subband images of the second decomposition level are located in the upper left 32a, upper right 32b, lower left 32c and lower right 32d quadrants of the upper left quadrant 30a. The coefficients produced by further decomposition may be arranged in a similar manner. For example, for a third level of decomposition, the upper left quadrant 32a includes the wavelet coefficients of the LL, LH, HL and HH subbands of the third decomposition level. Specification, pp. 6-7.

If the coefficient matrix that indicates the pixel intensities for the original image is a 4X4 matrix, then the matrix 40 may be of the form that is depicted in Fig. 5. In this manner, the LL, LH, HL and HH subband images of the second decomposition level each have one coefficient, represented by "A" (for the LL subband image), "B" (for the LH subband image), "C" (for the HL subband image) and "D" (for the HH subband image), respectively. As depicted in Fig. 5, for the first decomposition level, the coefficients for the LH, HL and HH subband images are represented by the following respective matrices:

$$\begin{bmatrix} E_1 & E_2 \\ E_3 & E_4 \end{bmatrix}, \begin{bmatrix} F_1 & F_2 \\ F_3 & F_4 \end{bmatrix}, \begin{bmatrix} G_1 & G_2 \\ G_3 & G_4 \end{bmatrix}$$

It is noted that each coefficient of the second decomposition level (except A), is associated with at least four coefficients of the first decomposition level, i.e., each coefficient of the first decomposition level has at least four descendant coefficients in the second decomposition level. Therefore, each bit in the first decomposition level has at least four descendent coefficients in the second decomposition level. Specification, p. 7.

For each bit order, the processor 112 may process the bits in the scanning sequence described above. If a particular bit indicates a "1" or a "-1," then the processor 112 generates the P or N code and proceeds to process the next bit in the scanning sequence. However, if a particular bit indicates a "0," then the processor 112 may trace the bit through its descendants to determine if the bit is an isolated zero or a zerotree root. The coefficients in the LL subband are simply entropy encoded. Specification, pp. 7-8.

As an example, to produce the code for the least significant bit (called D(1)) of the D coefficient (located in the HH subband of the second decomposition level), the processor 112 determines whether the D(1) bit indicates a "0." If so, the processor 112 evaluates the descendant bits $G_1(1)$, $G_2(1)$, $G_3(1)$ and $G_4(1)$ of the subband HH of the first decomposition level in search of a "1" or "-1," as indicated in Fig. 6. If one of these bits indicates a "1" or "-1," then the D(1) bit is an isolated zero. Otherwise the D(1) bit is a zerotree root. Specification, p. 8.

As a numeric example, a 4X4 coefficient matrix that indicates pixel intensities for an image may undergo a two level decomposition to form the following matrix:

$$\begin{bmatrix} 4 & 1 & 1 & 2 \\ -2 & 0 & 0 & 1 \\ 0 & 3 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

Because the maximum absolute value is "4," three bits may be used to represent the coefficients, as depicted in the following matrix:

$$\begin{bmatrix} 100 & 001 & 001 & 010 \\ -010 & 000 & 000 & 001 \\ 000 & 011 & 000 & 000 \\ 000 & 001 & 000 & 000 \end{bmatrix}$$

Therefore, the processor 112 begins the encoding by generating codes for the third order bits (i.e., the most significant bits, which may be zero also) of the coefficients. More particularly, to generate the codes for the third order bits, the processor 112 follows the path 28 (see Fig. 5) and produces the appropriate code for the third bit of each coefficient along the path 28. If a particular bit indicates a "0," then the processor 112 evaluates the descendants of the bit to find isolated zeros and zeroroots. The coding of the third order bits by the processor 112 produces the following codes (listed in the order of production): P,R,R,R. Subsequently, the processor 112 produces the codes for the second order bits (listed in order of production): IZ,IZ,N,R,IZ,P,IZ,IZ,IZ,P,IZ,IZ. Lastly, the processor 112 produces the codes for the first order bits (listed in order of production): IZ,P,IZ,R,P,IZ,IZ,P,IZ,P,IZ,P. As described above, the processor 112 may indicate the codes via a two bit coding scheme and transmit the codes as produced via a bit stream. Specification, pp. 8-9.

As an example, another processor 200 (see Fig. 2) may use the bit stream to reconstruct the coefficient matrix that indicates the pixel in intensities of the original image in the following manner. Before the decoding begins, the processor 200 first receives an indication from the processor 112 that three levels of coding (i.e., one level for each bit order) have been used. After obtaining this information, the processor 200 may reconstruct the original coefficient matrix using the codes in the order that the codes are produced. More particularly, the processor 200 may use the codes produced by the coding of the bits of the third bit order (i.e., the first level of coding) to produce the following matrix:

$$\begin{bmatrix} 100 & 000 & 000 & 000 \\ 000 & 000 & 000 & 000 \\ 000 & 000 & 000 & 000 \\ 000 & 000 & 000 & 000 \end{bmatrix}$$

The processor 200 may use this matrix to reconstruct a coarse version (i.e., a lower resolution version) of the original image. However, if a more refined version is desired, the processor 200 may use the codes that are produced by the coding of the second bit order (i.e., the second level of coding) to produce the following matrix:

$$\begin{bmatrix} 100 & 000 & 000 & 000 \\ -010 & 000 & 000 & 000 \\ 000 & 010 & 000 & 000 \\ 000 & 000 & 000 & 000 \end{bmatrix}$$

Finally, if the processor 200 uses the codes that are produced by the coding of the bits of the first order (i.e., the third level of coding), the processor 200 produces the original matrix of decomposed wavelet coefficients. Specification, pp. 9-10.

Referring to Fig. 7, to summarize, the compression program 119, when executed by the processor 112 may cause the processor 112 to perform the following procedure to produce the above-described coding. First, the processor 112 may express (block 72) a matrix of decomposed coefficients in a signed binary representation. Next, the processor 112 may determine (block 74) the number of digits that are needed to represent the absolute value of the maximum wavelet coefficient. This processor 112 uses a variable (called n) that indicates the current bit order being processed by the processor 112. In this manner, the processor 112 uses a software loop to process the bits, one bit order at a time. To accomplish this, the processor 112 produces codes (block 76) for the bits of the current bit order the using the techniques described above. Subsequently, the processor 112 determines (diamond 78) whether the rate of transmitted bits may exceed a predetermined bit rate. If so, the processor 112 terminates the coding for the current image to comply with the predetermined bit rate. Otherwise, the processor 112 determines (diamond 80) if all bit orders have been processed, i.e., the processor 112 determines if n equals "1." If not, the processor 112 decrements (block 75) the order that is indicated by the n variable by one and proceeds to block 76 to traverse the loop another time to produce codes for the bits of another bit order. Otherwise, the coding is complete. Specification, p. 10.

Referring back to Fig. 2, in some embodiments, the processor 112 may be part of a computer system 100. The computer system 100 may include a bridge, or memory hub 116, and the processor 112 and the memory hub 116 may be coupled to a host bus 114. The memory hub 116 may provide interfaces to couple the host bus 114, a memory bus 129 and an Accelerated Graphics Port (AGP) bus 111 together. The AGP is described in detail in the Accelerated

Graphics Port Interface Specification, Revision 1.0, published on July 31, 1996, by Intel Corporation of Santa Clara, California. A system memory 118 may be coupled to the memory bus 129 and store the compression program 119. As described above, the compression program 119, when executed by the processor 112, may cause the processor 112 to provide wavelet coefficients that indicate an image and represent each wavelet coefficient as a collection of ordered bits. The processor 112 codes the bits of each order to indicate zerotree roots that are associated with the order. Specification, pp. 10-11.

Among other features of the computer system 100, a display controller 113 (that controls the display 114) may be coupled to the AGP bus 11. A hub communication link 115 may couple the memory hub 116 to another bridge circuit, or input/output (I/O) hub 120. In some embodiments, the I/O hub 120 includes interfaces to an I/O expansion bus 125 and a Peripheral Component Interconnect (PCI) bus 121. The PCI Specification is available from The PCI Special Interest Group, Portland, Oregon 97214. Specification, p. 11.

A modem 140 may be coupled to the PCI bus 121 to a telephone line 142. In this manner, the modem 140 may provide an interface that permits the bit stream that is produced by the processor 112 to be communicated to the processor 200. The I/O hub 120 may also include interfaces to a hard disk drive 132 and a CD-ROM drive 133, as examples. An I/O controller 117 may be coupled to the I/O expansion bus 125 and receive input data from a keyboard 124 and a mouse 126, as examples. The I/O controller 117 may also control operations of a floppy disk drive 122. Copies of the program 119 may be stored on, as examples, the hard disk drive 132, a diskette or a CD-ROM, as just a few examples. Specification, p. 11.

In the context of this application, the phrase "computer system" may generally refer to a processor-based system and may include (but is not limited to) a graphics system, a desktop computer or a mobile computer (a laptop computer, for example), as just a few examples. The term "processor" may refer to, as examples, at least one microcontroller, X86 microprocessor, Advanced RISC Machine (ARM) microprocessor, or Pentium-based microprocessor. The examples given above are not intended to be limiting, but rather, other types of computer systems and other types of processors may be included in embodiments of the invention. Specification, pp. 11-12.

## VI. ISSUES

**A. Can claims 16-22 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 16?**

**B. Can claims 23-28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 23?**

**C. Can claims 29-33 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 29?**

## VII. GROUPING OF THE CLAIMS

Claims 16-22 can be grouped together; claims 23-28 can be grouped together; and claims 29-33 can be grouped together. Furthermore, regardless of the grouping that is set forth by the Examiner's rejections, the claims of each group set forth in this section stand alone with respect to the claims of the other groups that are set forth in this section. In other words, any claim of a particular group that is set forth in this section does not stand or fall together with any claim of any other group that is set forth in this section.

## VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

### A. Can claims 16-22 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 16?

The method of claim 16 includes providing wavelet coefficients that indicate an image. The bits of each wavelet coefficient are associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient. For each bit order, the associated bits are coded to indicate the zerotree roots that are associated with the bit order.

The Examiner rejects independent claim 16 under 35 U.S.C. § 103(a) as being unpatentable in view of the combination of U.S. Patent No. 6,144,773 (herein called "Kolarov") and U.S. Patent No. 6,222,941 (herein called "Zandi"). Zandi generally teaches an apparatus for compression using reversible embedded wavelets.

More specifically, Zandi teaches zerotree encoding multibit wavelet coefficients, not representing each wavelet coefficient as a collection of ordered bits and coding the bits of each order to indicate zerotree roots that are associated with the order. Thus, claim 16 is directed to a bitwise zerotree coding scheme, and in contrast, Zandi is directed to a coefficient-based zerotree coding scheme. The Examiner refers to the language in Zandi that begins on line 59 of column 22 and ends on line 25 of column 27. However, this discussion relates to zerotree encoding wavelet coefficients, not coding bits of each bit order to indicate zerotree roots that are associated with the bit order. Although beginning on line 27 of column 24 Zandi teaches determining whether a particular wavelet coefficient is a zerotree root based on a most

significant bit $S_A$, Zandi neither teaches nor suggests coding the bits of each bit order. In this manner, this language of Zandi teaches analyzing the most significant bit of a particular wavelet coefficient to determine whether the coefficient should be classified in what Zandi calls an A-group or a B-group. However, Zandi does not teach or even suggest coding the bits of each bit order to indicate zerotree roots that are associated with the order.

In general, Kolarov is directed to wavelet-based data compression. Figs. 3A and 3B of Kolarov depict one compression technique; and Figs. 4A-4C depict another compression technique. In block 309 of Fig. 3A, Kolarov mentions identifying a number of bit planes. Also, in Fig. 3A, Kolarov shows a block 320 in which data analysis is performed to calculate wavelet coefficients. The corresponding text appears in lines 36-43 in column 12 and in lines 53-61 in column 13 of Kolarov. However, neither in Fig. 3A, the text that corresponds to Fig. 3A nor elsewhere in Kolarov does Kolarov teach or suggest coding the bits of each bit order to indicate zerotree roots that are associated with the order.

The combination of Zandi and Kolarov fails to teach or suggest coding associated bits to indicate zerotree roots that are *associated with the bit order*. (emphasis added). It is first noted that Zandi fails to teach or suggest these claim limitations. More specifically, Zandi is directed to *zerotree encoding multibit coefficients*, not coding associated bits of each bit order to indicate zerotree roots that are associated with the bit order. Thus, the Examiner relies on Kolarov to allegedly teach the missing claim limitations. However, Kolarov also fails to teach or suggest the missing claim limitations. The Examiner, in fact, states that these claim limitations are not explicitly recited in Kolarov. Final Office Action, 3. However, the Examiner proceeds to

selectively read portions of Kolarov to allegedly support the conclusion that Kolarov teaches zerotree encoding of bit orders. More specifically, the Examiner refers to Figs. 4A-4C and the corresponding text in Kolarov in an attempt to show that Kolarov somehow implicitly or inherently teaches wavelet encoding of bit orders. However, Figs. 4A-4C and the corresponding text in Kolarov simply teach testing wavelet coefficients for bit significance. Testing a wavelet coefficient for bit significance is not equivalent to encoding the bit orders of wavelet coefficients. This language of Kolarov is, contrary to the Examiner's contentions, directed to encoding entire multiple bit wavelet coefficients for zerotree roots, not for each bit order, coding associated bits to indicate zerotree roots that are associated with the bit order. Thus, the Examiner fails to show where Kolarov implicitly teaches coding bits of wavelet coefficients to indicate zerotree roots for the bit orders. The missing claim limitations are not inherent in Kolarov, as these claim limitations do not *necessarily flow* from Kolarov. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). More specifically, there is a clear alternative to encoding zerotree roots for bit orders: encoding zerotree roots for entire wavelet coefficients. Thus, the missing claim limitations are not inherent in Kolarov.

"Obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966). Thus, in order to establish a *prima facie* case of obviousness, the Examiner must show that one skilled in the art, without knowledge of the claimed invention, would have derived the claimed invention in view of Zandi and Kolarov. The Examiner has failed to make this showing, as the Examiner is selectively reading these references in view of the Examiner's knowledge of the claimed invention.

Claims 17-22 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 16-22 are improper and should be reversed.

**B. Can claims 23-28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 23?**

The article of claim 23 includes a storage medium that is readable by a processor-based system. The storage medium stores instructions to cause a processor to provide wavelet coefficients that indicate an image. The bits of each of wavelet coefficient are associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient. The storage medium stores instructions to cause the processor to for each bit order, code the associated bits to indicate the zerotree roots that are associated with the bit order.

The Examiner rejects independent claim 23 under 35 U.S.C. § 103(a) in view of the combination of Zandi and Kolarov. However, this combination of references fails to teach or suggest all claim limitations. For example, neither Zandi nor Kolarov teaches or suggests instructions to cause a processor to for each bit order, code associated bits to indicate zerotree roots that are associated with the bit order. Instead, Zandi and Kolarov are directed to encoding zerotree roots for multibit wavelet coefficients, not encoding zerotree roots for each bit order. The Examiner contends that although Kolarov does not explicitly teach the missing claim limitations, Kolarov somehow implicitly or inherently teaches these claim limitations. Final Office Action, 3.

However, the Examiner fails to show the language that allegedly, implicitly or inherently teaches the missing claim limitations. For a claim limitation to be inherent, the claim limitation must *necessarily flow* from the cited reference. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). This is not the case here, as a clear alternative is zerotree encoding the multibit wavelet coefficients themselves instead of zerotree encoding the bit order. The Examiner points to no text that would imply the missing claim limitations. Therefore, a *prima facie* case of obviousness has not been established for claim 23.

Claims 24-28 are patentable for at least the reason these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 23-28 are improper and should be reversed.

**C. Can claims 29-33 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 29?**

The computer system of claim 29 includes a processor and a memory. The memory stores a program to cause the processor to provide wavelet coefficients that indicate an image. The bits of each wavelet coefficient are associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient. For each bit order, the program causes the processor to code the associated bits to indicate zerotree roots that are associated with the bit order.

The Examiner rejects independent claim 29 under 35 U.S.C. § 103(a) in view of the combination of Zandi and Kolarov. However, the combination of these references fails to teach or suggest a program that causes a processor to for each bit order, code associated bits to indicate zerotree roots that are associated with the bit order. Instead, both Zandi and Kolarov are directed

to encoding zerotree roots for multiple bit wavelet coefficients, not encoding zerotree roots for particular bit orders. The Examiner admits that Kolarov does not explicitly teach the missing claim limitations and fails to show where Zandi teaches or suggests the missing claim limitations. Furthermore, the Examiner fails to support the contention that Kolarov allegedly implicitly or inherently teaches the missing claim limitations. Thus, a *prima facie* case of obviousness has not been established for independent claim 29.

Claims 30-33 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 29-33 are improper and should be reversed.

## IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: January 29, 2004

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## APPENDIX OF CLAIMS

The claims on appeal are:

16. A method comprising:

providing wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, coding the associated bits to indicate zerotree roots that are associated with said bit order.

17. The method of claim 16, wherein each bit order is associated with only one of the bits of each wavelet coefficient.

18. The method of claim 16, wherein the act of coding the bits comprises:

determining which of the bits indicate zeros; and

classifying each zero as either an isolated zero or a zerotree root.

19. The method of claim 18, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, and wherein the act of determining comprises:

traversing a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree roots.

20. The method of claim 16, wherein the act of providing comprises:

producing different levels of the code, each level being associated with a different resolution of the image.

21. The method of claim 20, wherein the levels that are associated with lower resolution are associated with higher orders.

22. The method of claim 16, wherein the act of providing wavelet coefficients comprises:

providing intensity level coefficients that indicate pixel intensities of the image; and

transforming the intensity level coefficients into wavelet subbands.

23. An article comprising a storage medium readable by a processor-based system, the storage medium storing instructions to cause a processor to:

provide wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, code the associated bits to indicate zerotree roots that are associated with said bit order.

24. The article of claim 23, wherein each bit order is associated with only one of the bits of each wavelet coefficient.

25. The article of claim 23, the storage medium comprising instructions to cause the processor to:

determine which of the bits indicate zeros, and

classify each zero as either an isolated zero or a zerotree root.

26. The article of claim 25, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, the storage medium comprising instruction to cause the processor to:

traverse a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree roots.

27. The article of claim 23, the storage medium comprising instructions to cause the processor to:

produce different levels of the code, each level being associated with a different resolution of the image.

28. The article of claim 27, wherein the levels that are associated with lower resolutions are associated with higher orders.

29. A computer system comprising:

a processor; and

a memory storing a program to cause the processor to:

provide wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, code the associated bits to indicate zerotree roots that are associated with said bit order.

30. The computer system of claim 29, wherein each bit order is associated with only one of the bits of each wavelet coefficient.

31. The computer system of claim 29, wherein the program causes the processor to code the bits by determining which of the bits indicate zeros and classifying each zero as either an isolated zero or a zerotree root.

32. The computer system of claim 31, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, and wherein the processor determines which of the bits are zeros by traversing a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree root.

33. The computer system of claim 29, wherein the program causes the processor to provide the wavelet coefficients by producing different levels of the code, each level being associated with a different resolution of the image.

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| Applicants: | Tinku Acharya, et al. | § | Group Art Unit: | 2625 |
| Serial No.: | 09/390,255 | § | Examiner: | Timothy M. Johnson |
| Filed: | September 3, 1999 | § | | |
| For: | Wavelet Zerotree Coding of Ordered Bits | § | Atty. Dkt. No.: | ITL.0210US (P7057) |

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF TRANSMITTAL

Dear Sir:

Transmitted herewith in triplicate is the Appeal Brief in this application. The Notice of Appeal was filed on January 26, 2004.

Pursuant to M.P.E.P. § 1208.02, there is no fee due for this Appeal, because the Examiner reopened prosecution after filing of the first Appeal Brief on October 23, 2002. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0210US).

Respectfully submitted,

Date: January 29, 2003

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Janice Munoz